LISTING OF CLAIMS:

1-3. (Cancelled)

4. (Currently Amended) An application specific integrated circuit comprising:

a processor;

an internal bus coupling signals to and from the processor at a first clock frequency, the internal bus comprising an Advanced Microcontroller Bus Architecture Advanced High-performance Bus;

a bridge coupling signals from said internal bus to an off-chip device operating at a second clock frequency, the second clock frequency being slower than the first clock frequency, said bridge comprising a clock divider having an input receiving said first frequency and an output providing a clock signal at said second clock frequency, a register storing and coupling data between said internal bus and said off-chip device, and ready control logic modifying a HREADY signal to delay read and write cycles on said internal bus to accommodate data transfers on said off-chip device at said second clock frequency;

a configuration register storing a variable identifying said second frequency; and,

~~The apparatus of Claim 3 further comprising~~ reset control logic maintaining an HRESETn signal to said off-chip device in an active state until said configuration register is loaded with said variable.

5. (Currently Amended) An application specific integrated circuit comprising;

a processor;

an internal bus coupling signals to and from the processor at a first clock frequency, the internal bus comprising an Advanced Microcontroller Bus Architecture Advanced High-performance Bus;

a bridge coupling signals from said internal bus to an off-chip device operating at a second clock frequency, the second clock frequency being slower than the first clock frequency, said bridge comprising a clock divider having an input receiving said first frequency and an output providing a clock signal at said second clock frequency, a register storing and coupling data between said internal bus and said off-chip device, and ready control logic modifying a HREADY signal to delay read and write cycles on said internal bus to accommodate data transfers on said off-chip device at said second clock frequency;

a configuration register storing a variable identifying said second frequency; and,

~~The apparatus of Claim 3 further comprising~~ bus access control logic suppressing an HBUSREQ signal from said internal bus when said second frequency is different from said first frequency.

6. (Currently Amended) An application specific integrated circuit comprising;

a processor;

an internal bus coupling signals to and from the processor at a first clock frequency, the internal bus comprising an Advanced Microcontroller Bus Architecture, Advanced High-performance Bus;

a bridge coupling signals from said internal bus to an off-chip device operating at a second clock frequency, the second clock frequency being slower than the first clock frequency,

said bridge comprising a clock divider having an input receiving said first frequency and an output providing a clock signal at said second clock frequency, a register storing and coupling data between said internal bus and said off-chip device, and ready control logic modifying a HREADY signal to delay read and write cycles on said internal bus to accommodate data transfers on said off-chip device at said second clock frequency;

a configuration register storing a variable identifying said second frequency; and,

~~The apparatus of Claim 3 further comprising~~ bus access control logic suppressing an HBUSGRANT signal from said off-chip device when said second frequency is different from said first frequency.

7-20. (Cancelled)

21. (New) A method for operating an application specific integrated circuit of the type having:

a processor;

an internal bus coupling signals to and from the processor at a first clock frequency, the internal bus comprising an Advanced Microcontroller Bus Architecture Advanced High-performance Bus;

a bridge coupling signals from said internal bus to an off-chip device operating at a second clock frequency, the second clock frequency being slower than the first clock frequency, said bridge comprising a clock divider having an input receiving said first frequency and an output providing a clock signal at said second clock frequency, a register storing and coupling data between said internal bus and said off-chip device, and ready control logic modifying a HREADY signal to delay read and write cycles on said internal bus to accommodate data transfers on said off-chip device at said second clock frequency; and

a configuration register storing a variable identifying said second frequency;

comprising maintaining an HRESETn signal to said off-chip device in an active state until said configuration registor is loaded with said variable.

22. (New) The method of Claim 21, further comprising suppressing an HBUSREQ signal from said internal bus when said second frequency is different from said first frequency.

23. (New) The method of Claim 21, further comprising suppressing an HBUSGRANT signal from said off-chip device when said second frequency is different from said first frequency.